REMARKS

Claims 5, 22, and 85 have been amended. No claims have been added. Claim 87 has been cancelled. Thus, claims 1-86 and 88 are pending.

Applicant's representative is grateful for the allowance of claims 1-4, 6-21, 23-83, and 88.

Claims 5, 22, and 85 stand rejected under 35 U.S.C. § 112, second paragraph, as being allegedly indefinite due to minor informalities. Claims 5, 22, and 85 have been amended as suggested in the Office Action. Consequently, the rejection to claims 5, 22, and 85 should be withdrawn. Claims 5 and 22 are now believed to be allowable.

Claims 84-87 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar (U.S. Patent No. 6,338,144). This rejection is respectfully traversed.

The present invention is directed to a high speed memory system. According to one aspect of the present invention, a memory system include the use of separate read and write clock signals. Further, a memory module having a plurality of memory devices includes plural read clock lines for supplying a read clock from each of the read clock lines to the plurality of memory devices. At the same time, a single write clock line is supplied to the memory module. The write clock line is provided to a write clock regeneration circuit, which generates multiple copies of the write clock signal. These multiple write clock signals are then respectively distributed to the plurality of memory devices in the memory module. Accordingly, claim 84 recites: "a plurality of data read clock lines for receiving and providing respective data read clock signals to said plurality of memory devices; a data write clock line for receiving a data write clock signal; and a data write clock regeneration circuit coupled to said data write clock line and said memory devices for respectively providing a plurality of regenerated data write clock signals to said memory devices."

Doblar is directed to a computer system using a low skew differential clock system to supply a clock signal to a synchronous memory unit. The differential clock signal is generated by a clock generator 12 and supplied to both a processor 10 and a memory controller 14. The differential clock signal is the propagated from the memory controller 14 to a fan-out buffer 16, and then supplied to one or more memory modules 18, 20. Fig. 1; Fig. 4; column 2, lines 8-16. Each memory module include plural memory devices. Once the differential clock signal has arrived on a memory module, it is provided to a clock buffer 34 (Fig. 5), which generates a single ended clock signal (CLK) from the differential clock signal (CK/#CK). It is this single ended clock signal (CLK) which is provided to the plural memory devices 32a, 32b, 32c on each memory module 18, 20.

The Office Action alleges that Doblar teaches a clock regeneration circuit at Fig. 2, element 26a. In fact, Fig. 2 element 26a is not a clock regeneration circuit. As noted in the specification, and as can be seen in Fig. 2, the element 26a is component of a fan-out circuit 16 used to distribute multiple copies of the differential clock signal to multiple memory modules. Further, element 26a is not a part of any memory module (as required by claim 84).

Doblar, however, does teach a clock regeneration circuit in the form of a clock buffer 34 (Fig. 5). As previously described, the clock buffer 34 accepts a differential clock signal (CK, #CK) and generates a single ended clock signal (CLK) which is supplied to plural memory devices (32a, 32b, 32c). The Office Action admits that Doblar fails to disclose the use of a clock regeneration circuit with respect to a write clock line. However, the Office Action cites column 4, lines 32-37 to justify the conclusion that it would be obvious to extend the generic clock regeneration circuit of Doblar to a memory device utilizing a write clock line.

Such a conclusion is incorrect. Column 4, lines 32-37 discloses that "Processor 10 may also provide signals for storing data within memory unit 18 to memory controller 14 via processor bus 22." Since the clock generator 12 generates the differential clock signal (CK, #CK), the only signals which can be generated by the processor would be a

write command. Thus, column 4, lines 32-37 merely support the fact that the memory system of Doblar is capable of writing a memory device. It is respectfully submitted that there is no teaching nor suggestion regarding the use of independent read and write clock signals and the use of a write clock regeneration circuit as required in the above-cited limitation from claim 84 in a memory system having independent read and write clock signals.

Claim 84 is therefore believed to be allowable over the prior art of record. Claims 85-87 depend on claim 84 and are also believed to be allowable over the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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